

Shenzhen Biqu Technology 3D Printer G0B1 Project



BIGTREETECH

BIGTREETECH_CB1_V2.2_220812_220812




BIGTREETECH

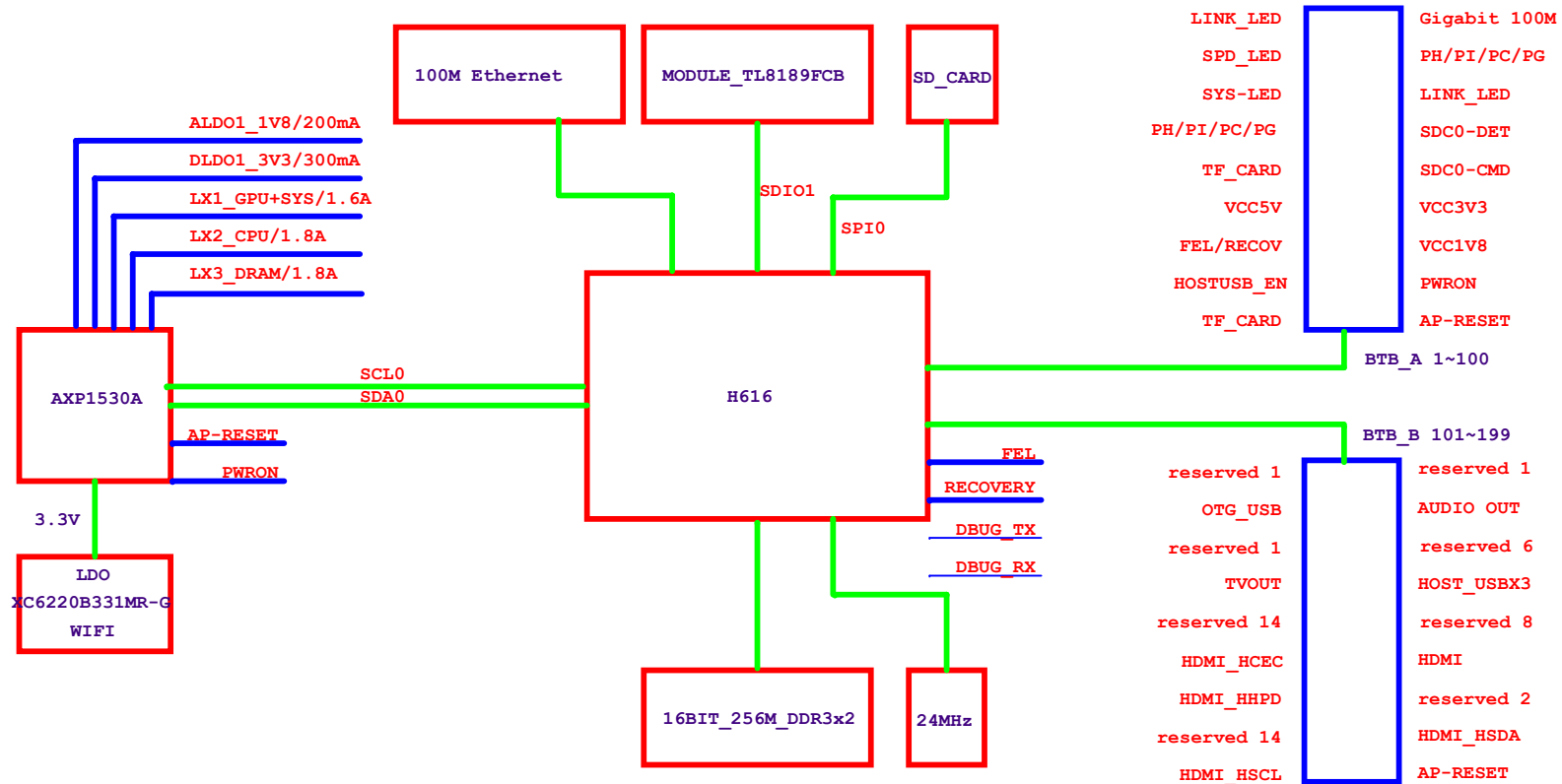
SOC: H616
 DDR: D2516ECMDXGJD
 MCU: STM32G0B1RCT6
 MODULE: TL8189FCB
 DCDC: AXP313A
 LDO: XC6220B331MR-G

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| Title | BIGTREETECH_CB1_V2.2 | |
| Design | Bron Bai | |
| Size | Document Number | Rev |
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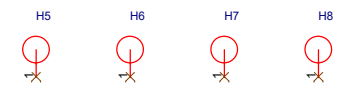
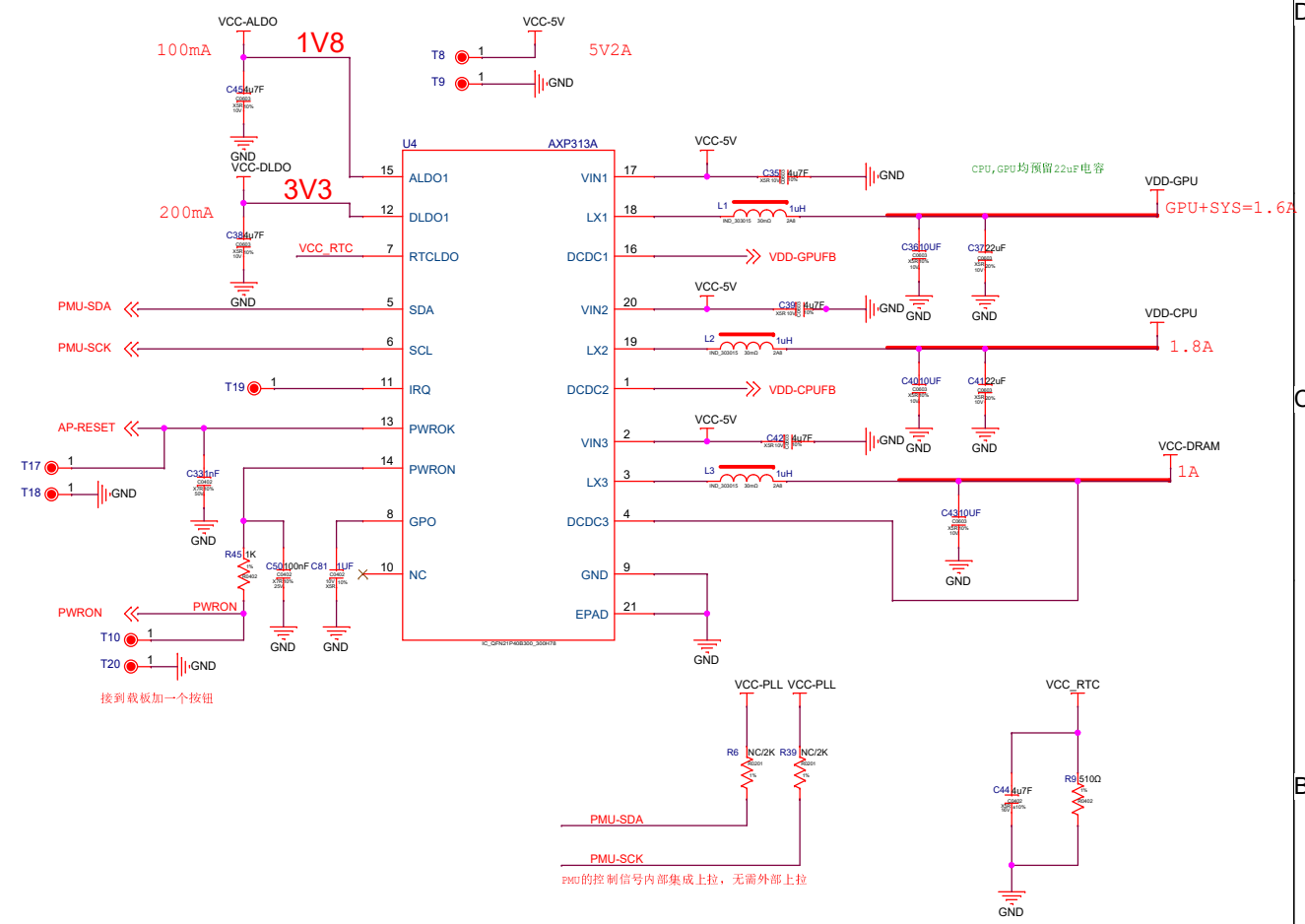
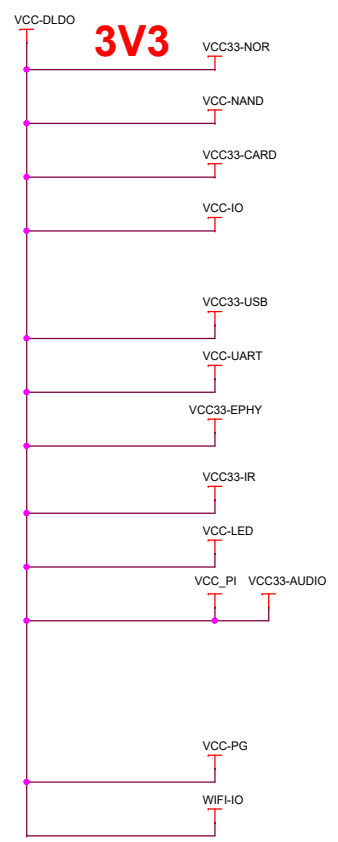
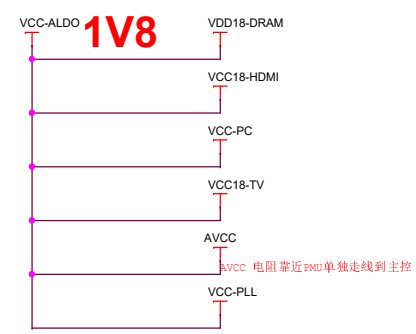
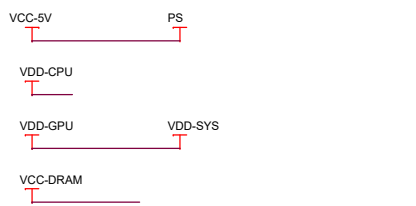
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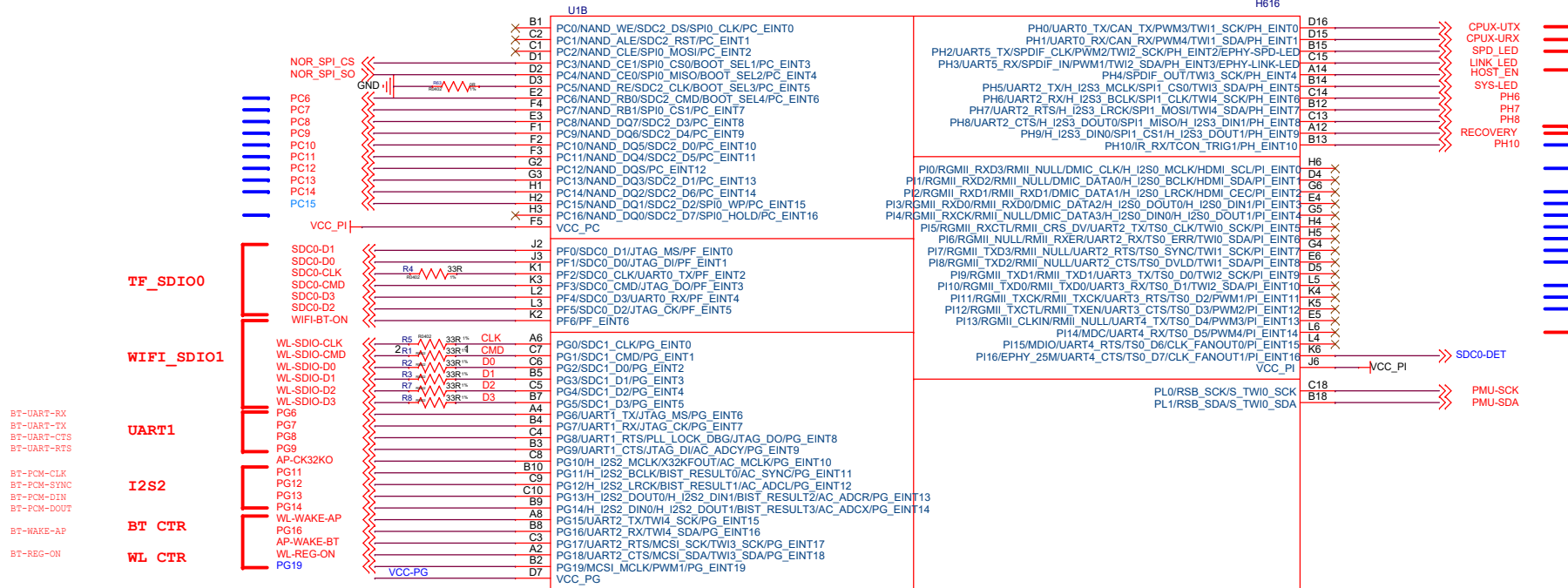
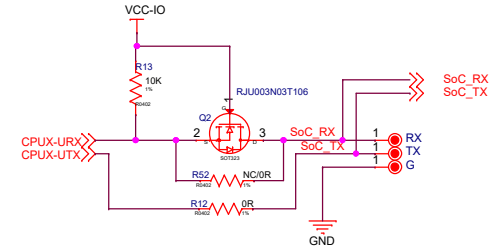
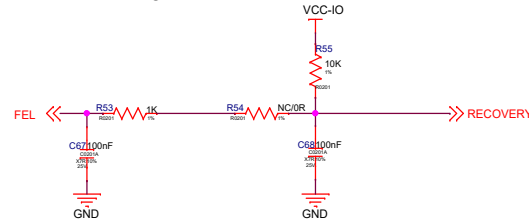
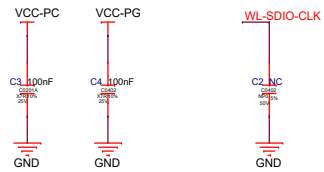


Version history

| Version | date | editor | Modify the description | approve |
|----------|------------|-----------|---|---------|
| 初始版本 | 2022.02.15 | Byron Bai | <ol style="list-style-type: none"> 在全志H616原始设计上修改。 取消EMMC, 用NORFLASH启动, 带TF卡。 WIFI改为模块TL8189FCB, 不带蓝牙。 增加两个BTB_DF40C-100DS-0-4V转接座子。 | |
| CB1_V1.0 | 2022.04.12 | Byron Bai | <ol style="list-style-type: none"> R43 要贴上,WIFI IO口用3.3v供电。取消掉R42, R43直连。 PC口 用1.8v.取消R40,3.3v的跳线: R41,1.8v跳线。 取消R44,用U5 RT9020-33GB直接供电给WIFI。 取消U7 MX25LI2835FM2I以及相关器件。 取消 R56 R11 R38版本设置电阻 1K。 取消IRQ_R62_OR.R70_OR。 取消WIFI_24_30PIN,取消WIFI 30P R51。 取消R60 R61 LDO分压 SoCB15 C15 网口灯取消,用PHY上面的灯控制口。 启动选择不要了。 取消A座 75P SD使能。 增加PHY RTL8211F和LDO供电。 修改更正SoC DDR IO的1.8v供电。 板名称BQ_G0B1_H616_CORE_V01_0221更改为BIGTREETECH CB1 V1.0 TF_CARD检测由“PI16”更换为“PI14”。 | |
| CB1_V2.0 | 2022.05.12 | Byron Bai | <ol style="list-style-type: none"> 取消TF_CARD检测“PI14”。 RGMII_MDC 由PI15更改到 PI14。 RGMII_MDIO 由PI16更改到 PI15。 R53,R54,R55,C67,C68,C27,C22,R10 封装更改为0201。 取消测试点T13,T14,T15,T16,T28。 Y1 24MHz封装更改为2012。 USB0 和USB1位置对调。 散热风扇控制更改为PC15。 | |
| CB1_V2.1 | 2022.06.08 | Byron Bai | <ol style="list-style-type: none"> 取消PHY YT8531。 改回内置100M网。 | |
| CB1_V2.2 | 2022.08.12 | Byron Bai | <ol style="list-style-type: none"> 删除了WIFI模块的丝印。 WIFI_LDO由RT9020-33GB更改为XC6220B331MR-G。 | |
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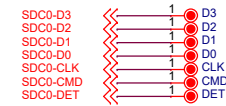


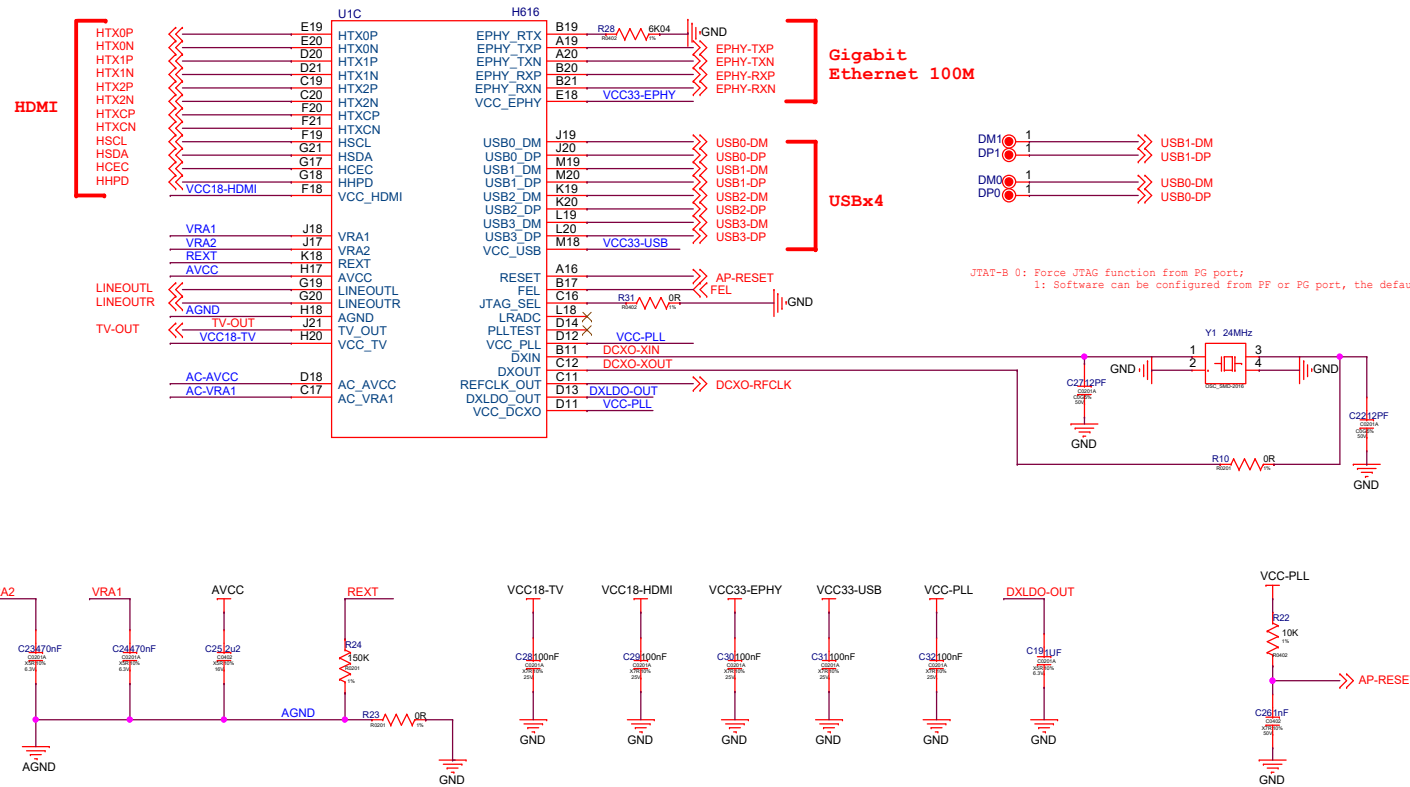
PMIC



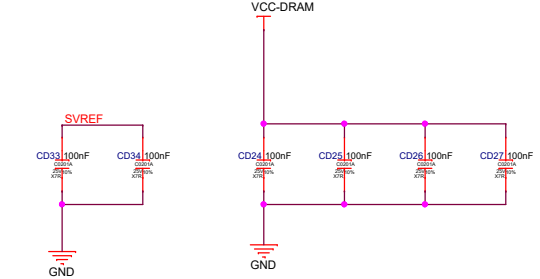
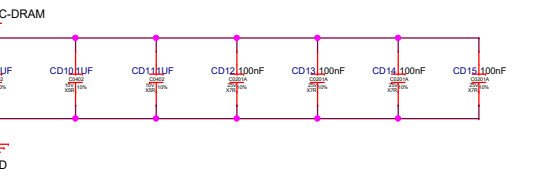
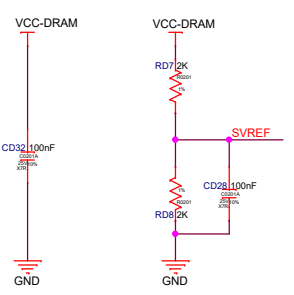
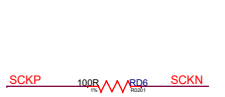
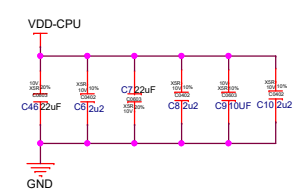
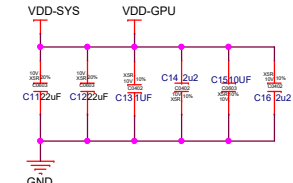
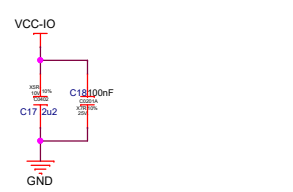
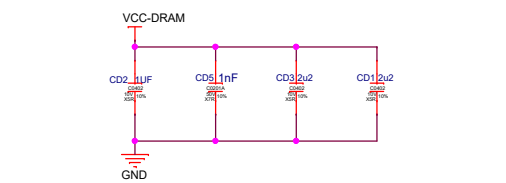
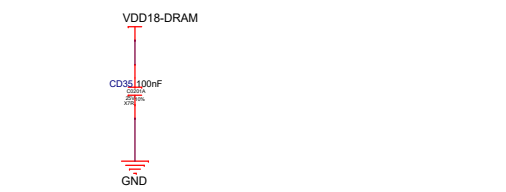
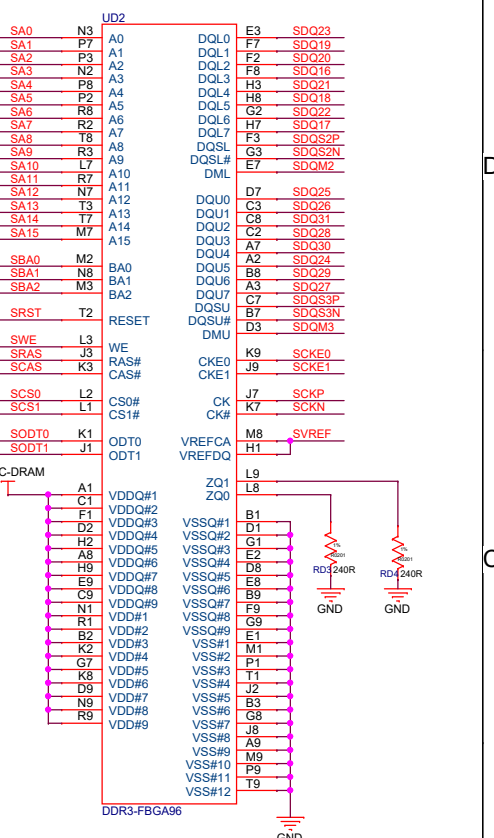
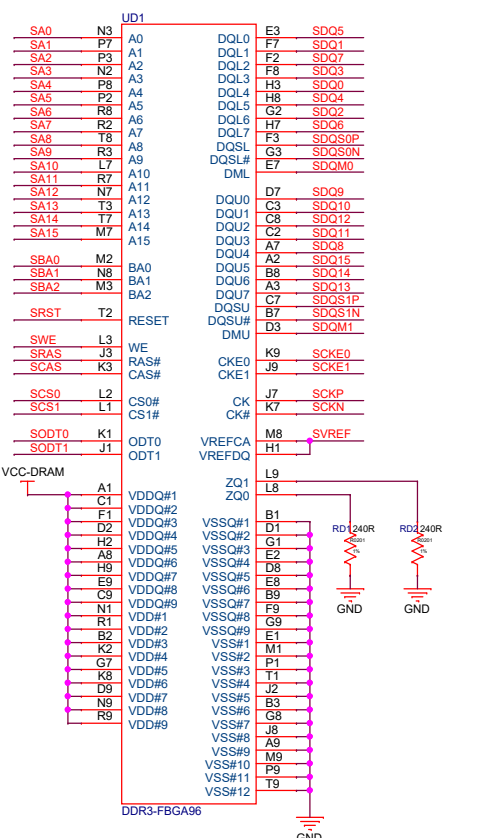
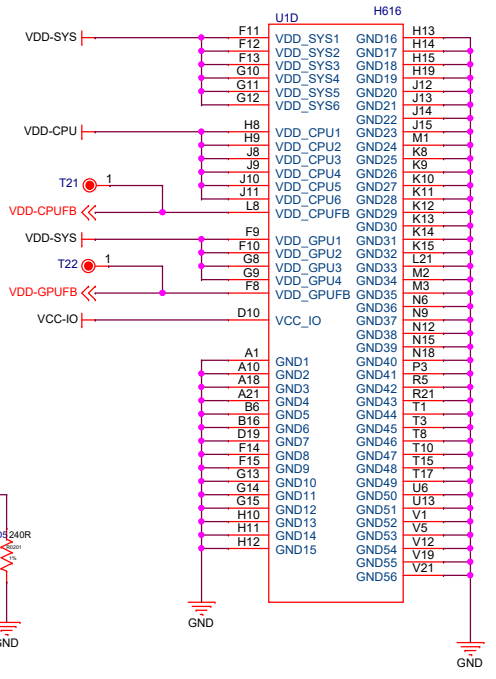
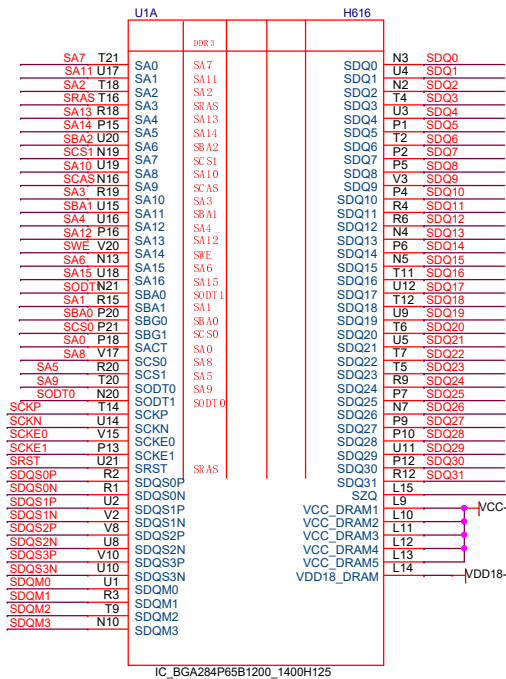
GPIO Instructions

- Note that the level of the SOC terminal matches the IO level of the peripheral
- The IO pull-up voltage selects the voltage of the power domain to which the corresponding GPIO belongs





JTAG-B 0: Force JTAG function from PG port;
 1: Software can be configured from PF or PG port, the default value of the register is PF.



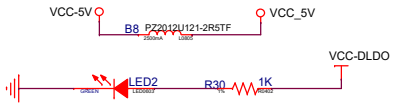
SOC_DDR3-CTRL

DDR3x2

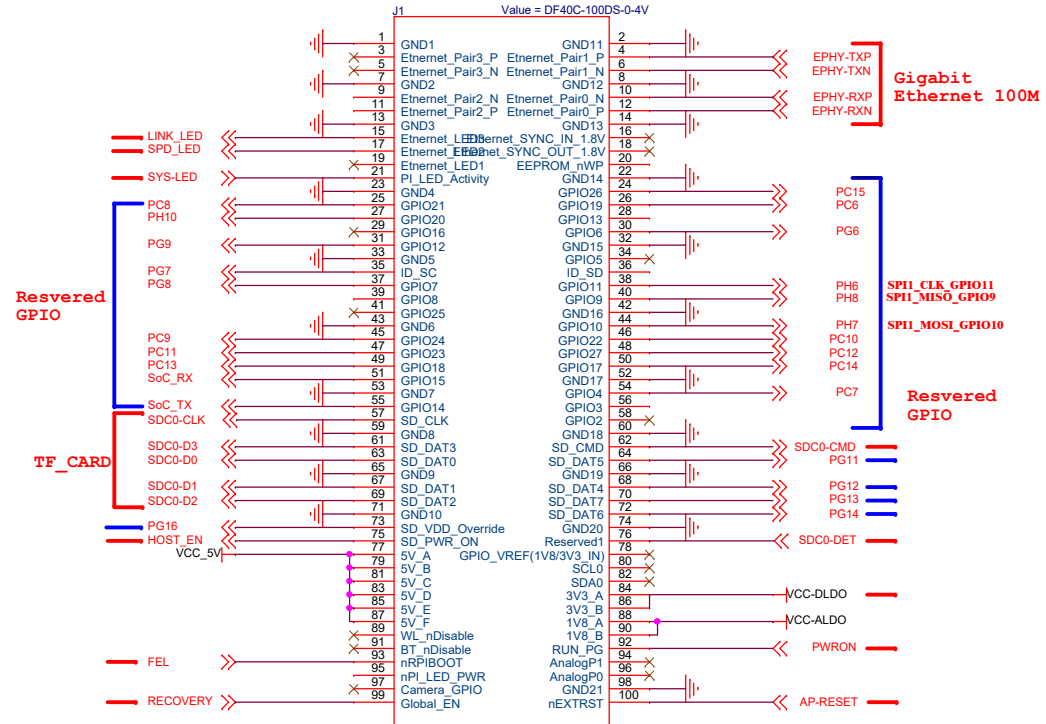
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| Title | BIGTREETECH_CB1_V2.2 | | Design |
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| Date | Thursday, September 15, 2022 | 08_Soc-DDRCTR_LPDDR3 32X1 | Rev |
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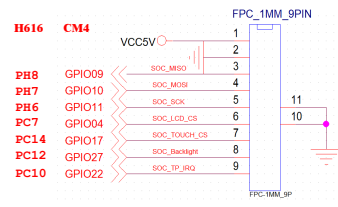


A 1~100



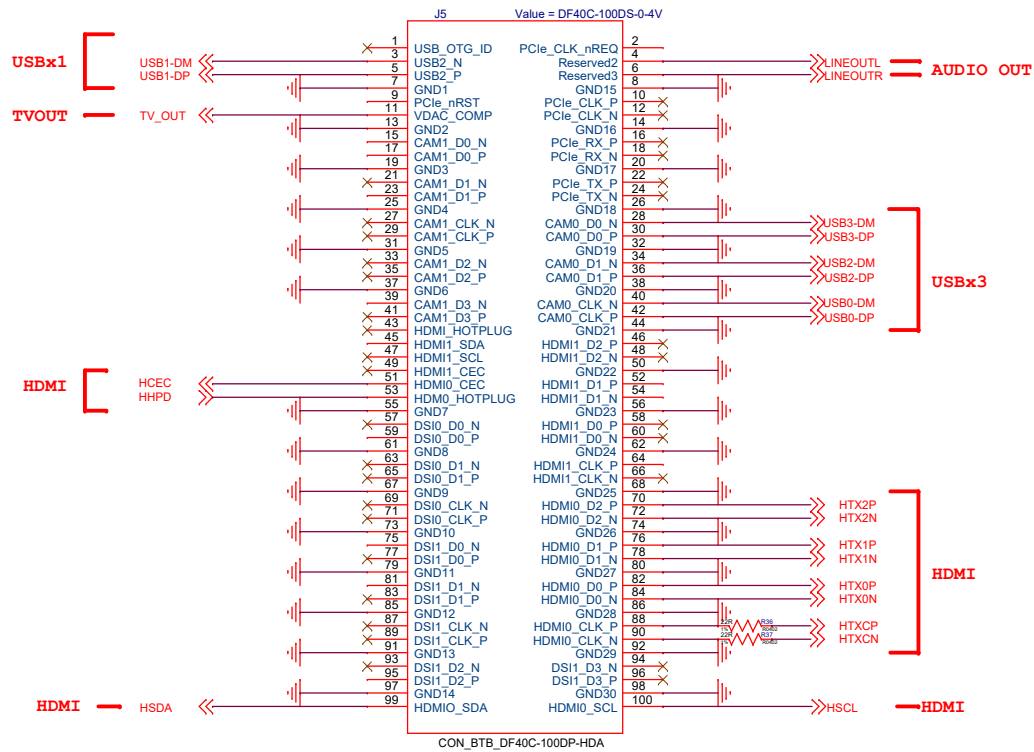
CON_BT_B_DF40C-100DP-HDA

A 1~100

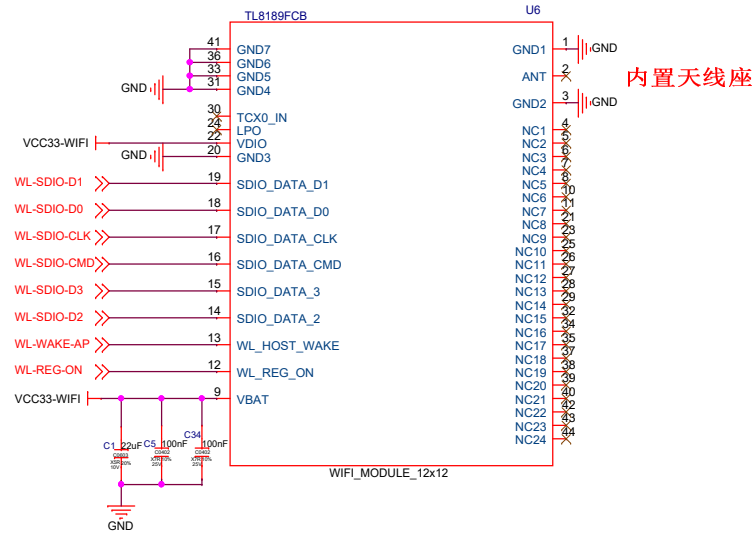


SoC_DISP

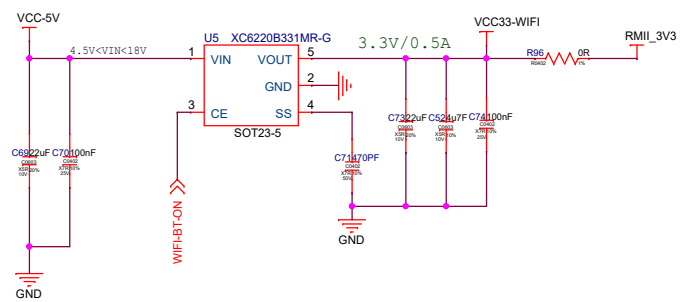
B 101~200



B 101~200



内置天线座



TL8189FCB_MODULE

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|---|------------------------------|
| Shenzhen Biqu Technology Co., Ltd. | |
| Title | BIGTRETTECH_CB1_V2.2 |
| Size | A3 |
| Document Number | 11_BT-WIFI_MODULE |
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